EVALUATION OF THE EFFECT OF THERMAL COUPLING IN A TEMPERATURE-LIMITED POWER TRANSISTOR SWITCH ON THE DISTRIBUTION OF STATIONARY POWER DISSIPATION IN THE TRANSISTORS

V. A. Belyakov and V. V. Togatov

UDC 621.382.2.016.3

The average value and mean-square deviation of the dissipated power are obtained as a function of the thermal resistances of the couplings. Criteria are established for evaluating the optimum values of these resistances.

The electrical and heat processes in a single temperature-limited (TL) transistor were analyzed in [1]. However, parallel operation of these transistors in a power transistor switch (TL switch) requires special study, since the distribution of power dissipation among separate transistors in the TL regime will be greatly affected by the thermal coupling between transistors in the switch, and this effect can be evaluated quantitatively from computational or experimental values of the so-called thermal resistance couplings. In doing so, it is necessary to find the dependence of the statistical characteristics (average value and mean-square deviation) of the stationary power dissipated in a single transistor as a function of the thermal resistance couplings and it is necessary to establish the permissible values of these resistances.

We will consider a TL switch consisting of N transistors, and in addition, we will assume that N is large enough (not less than 30-50 units) so that we can describe the thermal and electrical processes in the switch statistically. In using the principle of superposition, the stationary distribution of excess temperatures (referred to in what follows simply as temperatures) Θ_i among the transistors in the switch can be described by a system of algebraic equations:

$$\Theta_i = P_i R_{ii} + \sum_{\substack{j=1 \\ j\neq 1}}^{N} P_j R_{ji}, \quad i = 1, 2, \ldots, N. \tag{1}$$

In the system of equations (1), all the thermal resistances are considered to be independent of the power dissipated and the temperature.

In order to obtain equations for the average values $\bar{\Theta}$ of the temperatures Θ_i, it is enough to add term by term the equations in the systems (1) and to divide the left and right sides of the equations obtained by N. Adding term by term all the equations in system (1), we obtain

$$\sum_{i=1}^{N} \Theta_i = \sum_{i=1}^{N} P_i \left(R_{ii} + \sum_{\substack{j=1 \\ j\neq i}}^{N} R_{ji} \right) = \sum_{i=1}^{N} P_i R_i. \tag{2}$$

It can be shown that in (2) R_i consists of the thermal resistances of the i-th transistor when it is ideally thermally insulated from the rest of the transistors and with the retention of the previous conditions of heat transfer into the surrounding medium. The thermal resistances R_i can be taken as the same with sufficient accuracy for all the transistors and equal to R_0, as a result of which Eq. (2) can be written in the form

$$\sum_{i=1}^{N} \Theta_i = R_0 \sum_{i=1}^{N} P_i . \tag{3}$$

Institute of Precision Mechanics and Optics, Leningrad. Translated from Inzhenerno-Fizicheskii Zhurnal, Vol. 39, No. 4, pp. 704-709, October, 1980. Original article submitted April 9, 1979.

0022-0841/80/3904-1125$07.50

Dividing both parts of expression (3) by N, we obtain a relation between the average values of the temperatures of the transistors $\bar{\Theta}$ and the stationary dissipated power $\bar{P}$:

$$\bar{\Theta} = \bar{P} R_0 . \tag{4}$$

It follows from (4) that in a transistor switch made of the same kind of transistor with thermal resistance $R_i = R_o$, the average value of their stationary temperatures is related linearly to the average values of the stationary dissipated power through the constant coefficient, independent of the thermal resistance couplings and equal to the thermal resistance R_o.

Let us now analyze the effect of the thermal resistance couplings on the distribution of stationary dissipated power (referred to in what follows as simply the dissipated power) for the transistors in the TL switch.

From the system of equations (1) it follows that the temperature of the i-th transistor can be represented as a sum of two terms:

$$\Theta_i = \Theta_{P_i} + \Theta_{bi} , \tag{5}$$

Furthermore, $\Theta_{P_i} = P_i R_{ii}$ represents the temperature of the i-th transistor, arising from the dissipated power P_i in this transistor, while $\Theta_{b\,i} = \sum_{j=1,\ j\neq i}^{N} P_j R_{ji}$ is the temperature background of the i-th transistor, created by the rest of the transistors in the switch.

In the TL switch, the posistor (critical thermal resistor) for each i-th transistor provides feedback between Θ_i and P_i, which is expressed with sufficient accuracy in the stationary regime by the following relations:

$$\text{if} \quad \Theta_i < \Theta_{cri}, \text{then} \; P_i = P_{0i} , \tag{6}$$

$$\text{if} \quad \Theta_i = \Theta_{cri}, \text{then} \; P_i = \frac{\Theta_{P_i}}{R_{ii}} = \frac{\Theta_{cri} - \Theta_{bi}}{R_{ii}} , \tag{7}$$

$$\text{if} \quad \Theta_i > \Theta_{cri}, \text{then} \; P_i = 0 . \tag{8}$$

In (6)-(8), $\Theta_{cr\ i}$ is the so-called critical temperature of the i-th posistor. After this temperature is attained and exceeded, the power dissipated in the i-th transistor is limited. The critical temperature of posistors shows a statistical scatter in the range $\Theta_{cr\ min} \leq \Theta_{cr\ i} \leq \Theta_{cr\ max}$, and in addition, the average value $\bar{\Theta}_{cr}$ and the mean-square deviation $\sigma\Theta_{cr}$ of the critical temperature are determined by the technical preparation of the posistors and are assumed to be known.

In (6), P_{oi} is the power dissipated in the i-th transistor, which is determined only by its electrical operational regime and has a statistical scatter in the range $P_{o\ min} \leq P_{oi} \leq P_{o\ max}$, the magnitude of which stems from the scatter in the parameters of the current–voltage characteristics of the transistors in the switch. We will assume that P_{oi} for the i-th transistor does not depend on the power dissipated by other transistors. When they are connected in parallel, this limitation reduces to the requirement that the collector voltage be independent of the total current in the switch, which is fulfilled in practice in the saturation regime and when the switch is short-circuited, i.e., during its most strenuous operational regime.

Let us examine the limiting, in the sense of the operation of the temperature limitation, operational regime of the TL switch. Assume that there is feedback between Θ_i and P_i in the TL switch. Then, in the stationary regime powers P_{oi} will be dissipated in the transistors in the switch and each transistor will have a temperature Θ_{oi}. If, now, we include feedback, then the stationary power dissipation and the temperature of the transistors in the switch will change, and in addition, depending on the ratios of the values of Θ_{oi} and $\Theta_{cr\ i}$, the TL switch will be in one of two limiting operational regimes.

1. For all transistors $\Theta_{oi} < \Theta_{cr\ i}$. Due to the statistical distribution of the values of Θ_{oi} and $\Theta_{cr\ i}$, the condition $\Theta_{oi} < \Theta_{cr\ i}$ for all transistors will be satisfied simultaneously for $\Theta_{o\ max} < \Theta_{cr\ min}$. In this case, according to (6), no transistor is found in the TL regime and in each of them a power in the range $P_{o\ min} \leq P_{oi} \leq P_{o\ max}$ is dissipated, and this power is determined only by the electrical operational regime of the switch and does not depend on its thermal state and, in particular, on the thermal resistance coupling. In

this case, the distribution of the temperatures Θ_{oi} completely satisfies, in accordance with Eq. (1), the statistical distribution of the dissipated power P_{oi} occurring in the TL switch.

2. For all transistors $\Theta_{oi} \geq \Theta_{cr\ i}$. Due to the statistical distribution in the values Θ_{oi} and $\Theta_{cr\ i}$, the condition $\Theta_{oi} \geq \Theta_{cr\ i}$ is satisfied simultaneously for all transistors for $\Theta_{o\ min} \leq \Theta_{cr\ max}$. In this case, according to (7) and (8), the switch passes into the regime of total TL, the temperature falls into the range $\Theta_{cr\ min} \leq \Theta i \leq_{cr\ max}$, and the dissipated power in the range $0 \leq P_i \leq P_{oi}$. If, in this case, the temperature of each transistor Θ_{oi} is equal to the corresponding critical temperature $\Theta_{cr\ i}$ (from relation (7) it follows that for this to happen the conditions $\Theta_{cr\ min} > \Theta_{b\ max}$ and $\Theta_{cr\ max} < P_{o\ min} R_{ii\ min} + \Theta_{b\ min}$ must be satisfied), then no transistor in the switch will have $P_i = 0$ and $P_i \geq P_{o\ min}$, and the power dissipated will lie in the range $0 < P_i < P_{o\ min}$. In this case (which we will refer to as the normal TL regime), the distribution of power dissipation P_i is completely in accordance with Eq. (1) (expressed relative to the power) having in the TL switch a statistical distribution of the critical temperature $\Theta_{cr\ i}$.

Thus, in the most important regime for the investigation, the regime of total TL in the power dissipation range $0 < P_i < P_{o\ min}$, the system of equations (1) can be used for statistical analysis of the effect of the thermal resistance couplings on the distribution of dissipated power over the transistors of the TL switch. In this work, we examine the influence of the presence and intensity of thermal couplings in the TL switch. This statement of the problem permits excluding the scatter of the values of the thermal resistance couplings, i.e., to assume that all the resistance couplings R_{ji} are the same and equal R_c. In this case,

$$\sum_{\substack{j=1 \\ j \neq 1}}^{N} R_{ji} = (N-1) R_c . \tag{9}$$

It follows from (2) and (9) with $R_i = R_o = \text{const}$ that for all transistors $R_{ii} = \text{const}$. Denoting $R_{ii} = R$, $\sum_{j=1,\ j \neq i}^{N} P_j \approx (N-1)\bar{P}$, and taking into account (9), we obtain from (1) for the normal TL regime

$$\Theta_{cri} = P_i R + \bar{P}(R_0 - R) . \tag{10}$$

Introducing the coefficient of thermal coupling

$$k_c = R_0 / R , \tag{11}$$

we obtain from (4) and (10)

$$P_i = \frac{\Theta_{cri}}{R_0} k_c - \frac{\bar{\Theta}_{cr}}{R_0}(k_c - 1) . \tag{12}$$

From (12), it is easy to obtain an equation for the mean-square deviation of the dissipated power

$$\sigma P = \frac{\sigma \Theta_{cr}}{R_0} k_c . \tag{13}$$

Substituting into (4) the value $\bar{\Theta} = \bar{\Theta}_{cr}$, we obtain an equation for the average value of the dissipated power

$$\bar{P} = \bar{\Theta}_{cr} / R_0 . \tag{14}$$

It follows from (13) and (14) that in the normal TL regime, the average value of the dissipated power is determined by the average value of the critical temperature and does not depend on the thermal resistance couplings; the mean-square deviation of the dissipated power changes in proportion to the thermal coupling coefficient k_c. Since the thermal resistance R can vary from $R = R_o$, corresponding to the absence of thermal coupling between transistors, to $R_N = R_o/N$, corresponding to ideal thermal coupling between transistors, it is easy to see from (11) that k_c varies in the range $\Theta \leq k_c \leq N$, and in addition, the smallest value of σP is observed with $k_c = 1$, i.e., in the absence of thermal coupling in the switch. It follows from (12) that in this case each i-th transistor dissipates a power that depends linearly on the statistical value of $\Theta_{cr\ i}$. As k_c increases, σP increases, which leads to the fact that after some value of k_c is exceeded, the power P_i goes beyond the limit of the

range of applicability of Eq. (12), the statistical distribution of P_i breaks down, and Eqs. (13) and (14) are no longer valid.

Let us now examine how the total TL regime with $k_c = N$ comes about, i.e., with ideal thermal coupling between transistors in the switch. In this case, the TL switch as a thermal system degenerates into a homogeneous body with thermal resistance R_N and temperature

$$\Theta = \sum_{i=1}^{N} P_i R_N , \tag{15}$$

and in addition, $\Theta_{cr\ min} \leqslant \Theta \leqslant \Theta_{cr\ max}$. It is clear that the term Θ_{P_i} is absent in Eq. (15), causing a scatter in the temperature of individual transistors, i.e., the temperature Θ represents the background temperature, which is the same for all transistors. It now follows from (6)-(8) that those transistors for which $\Theta_{cr\ i} \leqslant \Theta$, will be switched off, while each transistor for which $\Theta_{cr\ i} > \Theta$, will dissipate power P_{oi}. In what follows, in order to simplify the presentation (but without loss of generality in the basic conclusions) we will assume that $P_{oi} = P_o = \text{const}$. If we denote the number of transistors with $P_{oi} = P_o$ as M, then in Eq. (15) $\sum_{i=1}^{N} P_i = MP_o$. Since $R_N = R_o/N$, we can obtain from (15) and (4) an equation for the average value of the dissipated power

$$\bar{P} = \frac{M}{N} P_0 = \frac{\Theta}{R_0} . \tag{16}$$

From (16), we find that

$$\frac{M}{N} = \frac{\Theta}{P_0 R_0} . \tag{17}$$

On the other hand, the ratio M/N can be easily expressed in terms of the probability of the distribution of the critical temperature in the TL switch $p(\Theta_{cr})$:

$$\frac{M}{N} = \int_{\Theta}^{\infty} p(\Theta_{cr})\, d\Theta_{cr} . \tag{18}$$

From (17) and (18), we obtain the equation

$$\frac{\Theta}{P_0 R_0} = \int_{\Theta}^{\infty} p(\Theta_{cr})\, d\Theta_{cr} , \tag{19}$$

the solution of which gives the value of Θ and M/N for a given value of P_o.

Thus, it has been shown that in the case of ideal thermal coupling in the TL switch the average dissipated power, according to (16), is determined by the temperature $\Theta_{cr\ min} \leqslant \Theta \leqslant \Theta_{cr\ max}$ and with a relatively small difference in the values of $\Theta_{cr\ min}$ and $\Theta_{cr\ max}$ can be nearly the same as the average dissipated power in the absence of thermal coupling, determined according to (14).

Here, thermal couplings can have a large effect on the scatter in the values of P_i. In the case examined, all transistors are separated according to power level into groups with $P_i = 0$ and $P_i = P_o$ and TL occurs only due to the change in the number of transistors switched in. This TL regime is not useful for TL switches, since it limits only the temperature of the transistors, not limiting at the same time the amount of power dissipated by separate transistors, which can cause them to break down.

Comparison of the TL regimes examined, limited according to the level of thermal coupling, shows that the ideal TL regime occurs in the absence of thermal couplings between transistors in the TL switch, i.e., with a zero value for the thermal resistance coupling. In this case, we obtain the lowest scatter in the values of P_i and TL is realized due to the decrease in the power dissipated in each transistor. Unfortunately, it is practically impossible to eliminate completely the thermal couplings between transistors in the TL switch. However, in constructing a TL switch, it is necessary to strive to decrease them, and in doing so, in order to estimate the optimal value of the coupling coefficient [k_c], it is useful to choose as a criterion the ratio of the allowable mean square deviation [σP] for dissipated power for a given switch to the value σP at $k_c = 1$. In this case, from (13), we obtain

$$[k_c] = \frac{[\sigma P]}{\sigma\Theta_{cr}} R_0 . \qquad (20)$$

We note that an increase in the temperature of the medium has the same effect as an increase in the thermal coupling, as a result of which the coefficient $[k_c]$ must be determined with the maximum possible temperature of the medium for the conditions under which the TL switch is used.

NOTATION

N, number of transistors in the switch; Θ_i, excess temperature of the i-th transistor; Θ_{oi}, same, but the switch is not in the temperature-limited regime; $\Theta_{cr\ i}$, excess critical temperature of the posistor of the i-th transistor; $\bar{\Theta}$, and $\sigma\Theta$, average value and mean-square deviation of the excess temperature of the transistors in the switch; $\bar{\Theta}_{cr}$ and Θ_{cr}, same for the posistors in the switch; P_i, stationary dissipated power in the i-th transistor; P_{oi}, stationary dissipated power of the i-th transistor, stemming only from the electrical operational regime of the transistor and not depending on its thermal state; $\bar{P}$ and σP, average value and mean-square deviation of the stationary dissipated power in the transistor; R_i, thermal resistance of the i-th transistor when it is ideally thermally insulated from the rest of the transistors; R_o, same, with $R_i = \text{const}$; R_{ii}, thermal resistance of the i-th transistor taking into account the thermal coupling with the rest of the transistors; R, same, with $R_{ii} = \text{const}$; R_N, same, with ideal thermal coupling between transistors; R_{ji}, thermal resistance of the coupling of the j-th transistor with the i-th transistor; R_c, same, with $R_{ji} = \text{const}$; $k_c = R_o/R$, coefficient of thermal coupling between transistors.

LITERATURE CITED

1. V. A. Belyakov and V. V. Togatov, "Analysis of electrical and thermal processes in temperature-limited transistors," Inzh.-Fiz. Zh., 38, No. 3, 457-464 (1980).